CS-173 Fundamentals of Digital Systems, Spring 2025

No.	Week	Monday		Thursday	
		Lecture (2 x 45')	**Exercise/TP (2 x 45')**	**Lecture (1 x 45')**	**Exercise/TP (2 x 45')**
1	17-Feb-2025	Intro to the course; Number systems (unsigned, signed)	No exercises (1st lecture)	Two's complement addition, subtraction, multiplication	Exercises
2	24-Feb-2025	Fractional numbers (floating-point, low precision)	Exercises	No lecture (Mirjana absent)	Exercises
3	3-Mar-2025	(1) Fractional numbers arithmetic (2) Logic functions, logic gates, Boolean algebra	Exercises	Logic functions, logic gates, Boolean algebra (Contd.)	Exercises
4	10-Mar-2025	Logic synthesis	Exercises, Boolean algebra	Arithmetic circuits (Two's complement adders)	Exercises, logic synthesis
5	17-Mar-2025	No lecture (Mirjana absent); Intro to Logisim	Exercises, Logisim	Introduction to Verilog	Exercises, Logisim
6	24-Mar-2025	(1) Verilog for combinational circuits (2) Implementation technology	Exercises, Logisim	Implementation technology (Contd.)	Exercises, Verilog
7	31-Mar-2025	Sequential logic	Exercises, Verilog	Registers and counters, Verilog	Exercises, Verilog
8	7-Apr-2025	Timing analysis of synchronous circuits	Mock exam	Memories (video lecture, Mirjana absent)	Exercises, Verilog
9	14-Apr-2025	Finite state machines	**Midterm exam**	Examples of finite state machines in Verilog	Exercises, Verilog
		Spring Break		Spring Break	
10	28-Apr-2025	Examples: Swapping two registers, generate construct in Verilog	Exercises, Verilog	Introduction to processors	Exercises, Verilog
11	5-May-2025	RISC-V Registers and integer computations (video lecture)	Exercises, Verilog	No lecture (Mirjana absent)	Exercises, RISC-V assembly
12	12-May-2025	RISC-V Memory acess and control transfer instructions	Exercises, RISC-V assembly	RISC-V Assembler directives	Exercises, RISC-V assembly
13	19-May-2025	Single-cycle CPU implementation	Exercises, RISC-V assembly	Multi-cycle CPU implementation	Exercises, RISC-V assembly
14	26-May-2025	Finale	Mock exam	Bank holiday	